A 4 GS/s,1.8 V Multiplexer encoder based Flash ADC using TIQ Technique.

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Abstract— **Analog-to-Digital converters (ADC) are useful components in signal processing and communication systems. In the digital signal processing (DSP) low power and low voltage are of prime concern and it is challenging to design high speed mixed signal circuits. This paper describes the ultra high speed ADC design using a 2x1 multiplexer based encoder that is highly suitable and accurate. Speed is an important parameter that is enhanced by using 2x1 multiplexer encoding network. In this paper a 4-bit, 1.8 V, high speed, low power, and low voltage CMOS flash ADC for SoC applications has been proposed. The 4-bit Flash type ADC has been designed with a step size of 0.038125 V. The proposed ADC architecture utilizes the Threshold Inverter Quantization (TIQ) technique that uses two cascaded Complementary Metal oxide semiconductor (CMOS) inverters as a comparator. The high speed and low power TIQ flash ADC architecture is designed and simulated using level 3 spice models. The ADC is designed with a 4 bit resolution and is simulated in 0.12 µm standard CMOS that offers a high data conversion rate of 4 Giga Samples/sec. Differential (DNL) errors measured are between -0.174 LSB to +0.256LSB. The ADC consumes 6.2031 mW from a 1.8 V supply with dynamic range of 600 mV**.

Keywords— Analog to Digital Converter, Digital signal processing, System on Chip, Threshold Inverter Quantization

I. INTRODUCTION

In the design of mixed-signal and system on chip (SoC) applications, the analog-to-digital converter (ADC) is a key functional block which limits the performance and speed of the system. Nowadays there are different types of ADCs available, which depend on the type of applications. ADCs are mostly classified as of three main categories; depending on their speed of operation. The three types of ADCs are a low speed serial ADC, medium speed ADC and high speed ADC. The serial ADC has a very high resolution but they operate at lower conversion speeds. The high speed ADC's support the high speed operation, offering error free conversion at very high frequencies but have relatively low resolution. Based on various topologies, different types of ADC's are: 1) Flash ADC, 2) Sigma delta ADC, 3) Ramp counter ADC and 4) Successive approximation ADC [1]. The different topologies in ADC's are designed using different technologies, the three main types of technologies used in data converters are the CMOS technology, the bipolar technology, and the Gallium Arsenide (GaAs) technology. SiCMOS technology has CMOS devices that have high noise immunity and low static power consumption [2-5]. CMOS technology also allows a high density of logic functions on a chip. It is primarily for this reason that CMOS became the most widely used technology to be implemented in VLSI chips. The work in this paper focuses on designing a low power, high speed analog to digital converter. In order to achieve maximum possible speed, Flash ADC topology have been used. Further CMOS technology has been adopted in order to consume less power. Flash ADC is the fastest ADC of all the various topologies available. It works faster just because of its parallel comparator array that facilitates parallel data conversion. Flash ADC design has been widely defined, and has different architectures, resolutions, sampling rates, power consumptions, and a range operating temperatures. These features available in a flash ADC are of prime importance. The work in this paper mainly focuses on 4-bit resolution. One of the most important features of flash ADC is that it has a large power dissipation and large chip area. The power dissipation increases with the speed and resolution. This results in limitations for Flash ADC at higher resolution. For a high-speed application, resolution and power consumption are key parameters. Generally the resolution is kept fixed once the ADC is designed for a particular application. On the other hand the power dissipation by a data converter varies with the sampling rate or the rate of conversion of analog signal, higher power is consumed at higher speeds. It is desirable to design an ADC that can operate at higher speed and will consume less power. In designing the high speed ADCs, the various blocks of ADC play an important role in speed, power performance. The code converter block of the ADC affects the speed parameter in the order of GS/s. ROM encoder [7-8] and fat tree encoders [9] are usually employed as code converters but these converters require a '01' generator to convert thermometer code into the 1-out-of-n code and then into binary code. Due to two step conversion process these converters introduce a large propagation delay of the order of ns [10], resulting in the speed limitation of up to few MHz. The usual implementation of encoder has been read-only memory (ROM), programmable logic array (PLA) circuits, and Fat tree encoder[16-18]. ROM implementation as compared to Fat tree encoder implementation is easier [12], but both of the encoding networks limit the speed to few hundred MS/sec. Fat tree gives an improved speed at cost of higher power dissipation than ROM type. The 2x1 multiplexer encoder based flash ADC

which is implemented in this paper out performs all presented ADC's. Flash ADC when designed using a faster technology of inverter [6], this resulted in a design of a faster ADC having faster inverter known as threshold inverter quantization (TIQ) ADC. TIQ technology makes ADC very fast and provides high conversion speed, besides reducing power dissipation of the data converter. The 2x1 multiplexer if used can out performs both the encoding networks especially when used with TIQ type of comparator technique using powerful CMOS technology. The work in this paper is carried out for a 4-bit Flash type ADC implementation using a 2x1 multiplexer encoding network. Although ADCs with 6-bit, 8-bit and 10-bit resolution also had been presented. The Flash ADC in this work has been designed for a 4-bit resolution using standard 0.12 um CMOS technology and implemented using the efficient technique called TIQ for comparator design and multiplexer based encoding network. The figure 1 shows the block diagram of the 4-bit Flash ADC implemented using TIQ technique with 2x1 multiplexer based encoding network. Simulation results showed a large improvement in the performance parameters. This paper is organized as follows: section I provide the introduction, section II starts with the related work carried out in the field of 4-bit Flash ADC Design. Section III provides details about the design process of 4-bit TIQ ADC and discusses the variations and mismatch effects. Section IV provides the implementation details and depicts the results. Section V provide the conclusions and references are listed in the end.

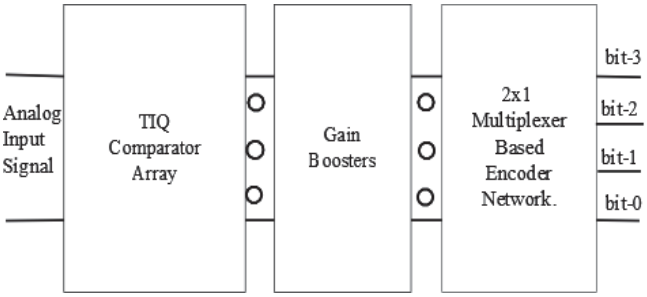

Figure1.Block Diagram of 2x1encoder based Flash ADC

II. Related Work

Traditionally high speed, and lower power conversion has been achieved by using different techniques and calibration methods. Design and implementation of an ultra-low-power, 4-bit 90nm CMOS Flash ADC based on gate-able comparators was carried out in [23], the design takes full advantage of comparator redundancy in order to achieve low power operation. With the power gating capabilities the design provides a peak speed of 2.5 GS/s only and consumes 30 mW of power. A 4-bit, 0.18 um, 2 GS/s flash ADC with 970.2 MHz input is presented in [24]. The analog part of this ADC in this work is fully pipelined, providing sampling rate of 2 GS/s only. It consumed 42 mW with a 1.8 V power supply. The work presented in [25], shows a low-power flash analog-to-digital converter (ADC) using logic gates as comparators. The work is more focused on reducing the static currents causing static power dissipations but speed parameters not have been taken into account. With the use of logic gate comparators, designers successfully reduced the static current typically up to 63 µA, and at 200 Mega sample per second (MS/sec), a conversion delay of 12.55 ns (~79.6 MHz) has been achieved. [26] proposes a CMOS technology based Flash ADC requiring 3.3 V supply, operating at 3-bit, 4-bit, 5-bit and 6-bit precision depending upon control inputs that change the resolution of data converter. The proposed data converter was designed in 0.35 um technology. The primary parameter considered here is Resolution, the work shows a design of a data converter which can work on 3-bit,4-bit,5-bit,6-bit resolution application but the speed and power dissipation are not considered as the proposed architecture was able to attain a maximum speed of 200 MS/sec only at max resolution. [27] describes a low power high speed 4-Bit TIQ based CMOS Flash ADC. The proposed design in it uses TIQ technique but implements the ADC using FAT tree type encoding network. The design is implemented using 0.12 µm process technology and is able to provide the conversion speed of 1GS/sec only. A different design is proposed in [28]. The work is carried out using standard CMOS technology of 45 nm. The ADC is best suitable for serial links in new communication technologies that require high speed but have ultra low power requirement, the input frequency for the said ADC is 1 GHz which results in a DNL of less than 0.5 LSB and INL less than 0.7 LSB and is within the acceptable limits to guarantee the monotonicity of the data converter. The complete ADC consumes less than 145 µwatts. It requires only 0.7 V supply voltage although at low power applications the ADC gives better performance but speed is still 1GHz only. This paper presents an ultrafast CMOS Flash A/D converter design. To achieve high speed in CMOS, the featured A/D converter utilizes the threshold inverter quantization (TIQ) technique and provides a conversion speed of 4 GS/s.

III. DESIGN.

A. Thereshold Inverter Quantisation

The comparator is the most important part of ADC. The TIQ technique is based on systematic transistor sizing of a CMOS inverter which eliminates the resistor array implementation of conventional comparator in the flash designs [1], [6]. This results in very lesser static power consumption, making it suitable for low power application. Each TIQ comparator is made of two cascaded comparators as shown in figure 2. The first inverter is designed with a unique threshold voltage for each step of input Voltage. The form factor for the CMOS inverter at first stage is appropriately selected and corresponding thereshold voltage for all TIQ comparators is set. The second inverter is designed with a constant form factor in order to have symmetric rise and fall times. The inverter threshold voltage Vm is defined as Vin = Vout in the voltage Transfer Characteristic (VTC) of an inverter. The Vm is internal to a comparator and is fixed for each comparator. The mathematical equation used to represent Vm is:

$$V_m = \frac{\left((V_{dd} - |V_{tp}| + V_{tn})\sqrt{\frac{k_p}{k_n}}\right)}{\left(1 + \sqrt{\frac{k_p}{k_n}}\right)} \qquad (1)$$

where V_{tp} and V_{tn} represent the threshold voltages of the PMOS and NMOS devices respectively And

$k_p = (W/L)_p . \mu_p . C_{ox}$

$k_n = (W/L)_n . \mu_n . C_{ox}$

Where W_p and W_n are the widths of PMOS and NMOS respectively. μ_p and μ_n are the hole and electron mobility respectively. C_{ox} is the gate oxide thickness, L the channel length of devices. The equation 1 is derived by assuming that

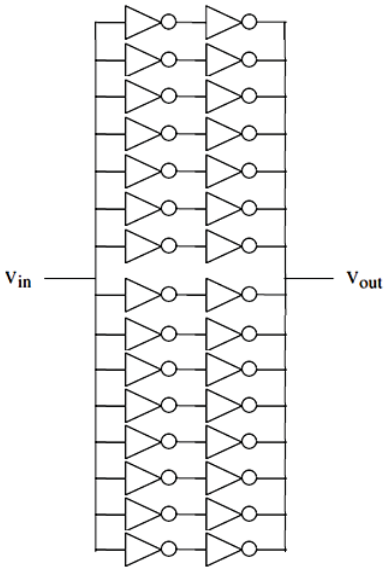

Figure 2.TIQ Comparators for 4 bit ADC

both the transistors operate in active region. Gate oxide for both devices is same. Lengths of the devices (L_p and L_n) is also fixed. From the equation 1 we can see that increasing width of NMOS makes V_m smaller and increasing width of PMOS makes V_m larger [4]. Hence with the fixed channel length of the both devices, we can get the desired threshold voltage of an inverter by simply changing the MOS shape factor or aspect ratio (S), S = W/L of the devices used. Since the length is not a degree of design freedom in the design methods, hence the widh of the devices i.e the widths of the PMOS and NMOS transistors are changed in order to achieve a desired threshold voltage. The design can also show degraded performance because of the variations in the threshold voltage of a comparator resulted due to the fluctuations in the supply voltage. Smaller fluctuations in the supply voltage of order of ±6 mV can show a marked variation in threshold voltage as shown in the figure 3. For the 0.12 µm technology with a nominal temperature of 27 ^oC and supply voltage of 1.8 V, V_{th}

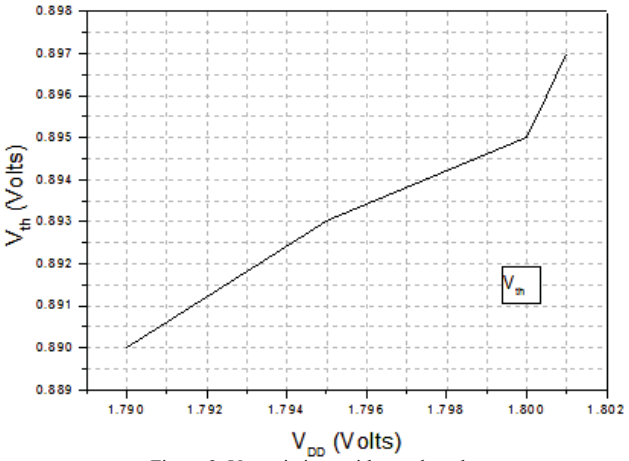

Figure 3. V_{th} variations with supply voltage.

for the designed comparator has an average value of 0.8956 volts and a standard deviation of 24.99 mV. It is observed that with ±0.5% change in the supply voltage of the data converter there is a ±0.27% change in the value of threshold voltage

B. TIQ Comparator

Comparator is a key design component of ADC. A total of (2^n-1) differential amplifiers working as comparators are required for an n-bit ADC. Design methods and the automation of the comparator circuit layout generation for a flash A/D converter are has been reported in [29]. TIQ comparator role is to convert an input voltage (Vin) into logic '1' or '0' by comparing a reference voltage (Vref) with Vin .When the input signal voltage is less than the reference voltage, then the comparator output is at logic '0'. When the input signal is higher than the reference voltage, the comparator output is at logic '1'. Comparator gives 2n-1 levels of output for reference voltage. The Flash ADC performance depends on comparator input signal without jitter [21].Therefore, this comparator consists of differential amplifiers. In this design, low leakage current MOS devices are used in order to keep the power consumption as small as possible. The sizes of the NMOS and PMOS transistors used in the proposed architecture of flash ADC corresponding to the minimum and maximum threshold voltages are shown in table I.

C. Gain Booster

The gain-boosting technique improves accuracy of the cascaded CMOS circuits without any speed penalty. This can be achieved by increasing the effect of the cascade transistor by means of an additional gain stage. Gain boosting stage consists of two cascading inverters with same circuit as comparator, except that the transistor sizes of each gain booster are smaller and identical to each other. The gain boosters make sharp thresholding of comparator output and provide full digital output voltage swing. The sizes of gain boosters are determined to obtain low rise and fall times.

TABLE I: SIZES OF THE TRANSISTORS FOR THRESHOLD VOLTAGES OF4-BIT FLASH ADC

Comparator	Vthreshold (Volts)	Wn (µm)	Wp (µm)
1	0.5000	0.384	0.206
2	0.538125	0.325	0.200
3	0.57625	0.282	0.200
4	0.614375	0.218	0.200
5	0.6525	0.2465	0.200
6	0.690625	0.19295	0.200
7	0.72875	0.171	0.200
8	0.766875	0.240	0.318
9	0.80500	0.210	0.312
10	0.843125	0.210	0.35
11	0.88125	0.210	0.393
12	0.919375	0.200	0.42
13	0.9575	0.200	0.472
14	0.995625	0.190	0.501
15	1.03375	0.180	0.537

IV. IMPLEMENTATION DETAILS.

A. 2x1 multiplexer based encoder architechture.

For an N-bit flash ADC the most significant bit (MSB) of binary output is high if more than half of the outputs in thermometer scale are at logic 1 [22]. Hence MSB is same as thermometer output at level 2N-1. To find the value at second most significant bit (MSB-1), original thermometer scale is divided into two partial thermometer scales, separated by output level at 2N-1. The partial thermometer scale to decode is chosen by a set of 2:1 Multiplexers where previous decoded binary output is connected to the control input of multiplexers. MSB-1 is then found from chosen partial thermometer scale in the same way as MSB was found from the full thermometer scale.

The chosen scale contains information about MSB-1, i.e. lower partial thermometer scale if output at level 2N-1 is logic. 0, otherwise upper partial thermometer scale is used. This is continued recursively until only one 2:1 multiplexer remains. Its output is least significant bit of binary output. Due to its regular structure, it can easily be expanded to operate in a system of higher resolution than 5-bits. A 5-bit multiplexer-based decoder is shown in Figure 4, which is built by 2:1 multiplexers and inverters.

B. Results and discussion

The proposed TIQ flash ADC has been designed with standard CMOS technology parameters keeping length of channel equal to 0.12 µm, with 1.8V supply. The encoder used is shown in

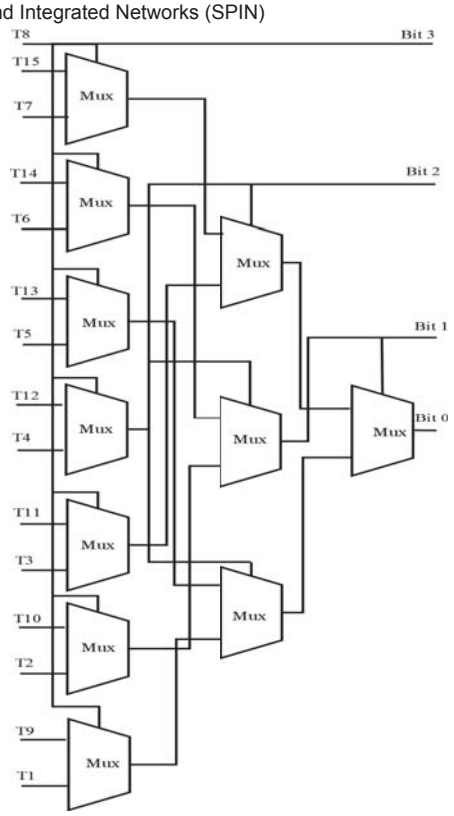

Figure 4 .Implementation of 2x1 Multiplexer based encoder

figure 4, HSPICE model (BSIM3) has been used for the experimental simulations. All the simulations are carried in Agilent Advanced Design system 2009. The output of the comparator array is shown in figure 5. The simulation of TIQ flash ADC output for a highly linear ramp input and a sinusoidal input signal are shown in figure 6 and figure 7 respectively. The total power dissipation by the TIQ flash ADC using the 2x1 multiplexing encoding network is shown in figure 8. Simulation results showed the power dissipation for the proposed architecture resulted in 6.2013 mW. Figure 9

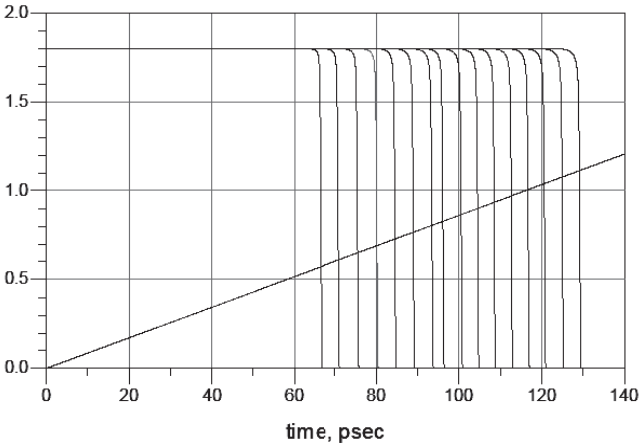

Figure 5. output of TIQ comparators with ramp input

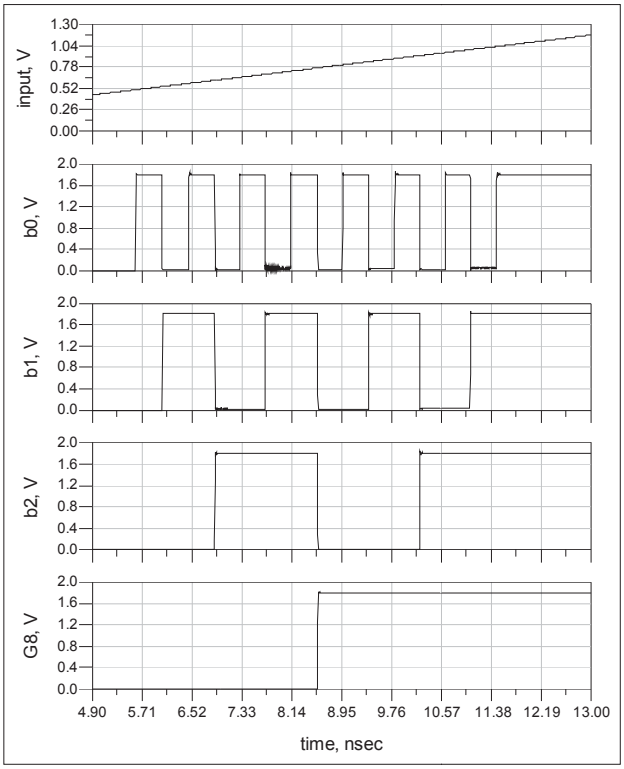

Figure 6. Transient analysis with ramp input.

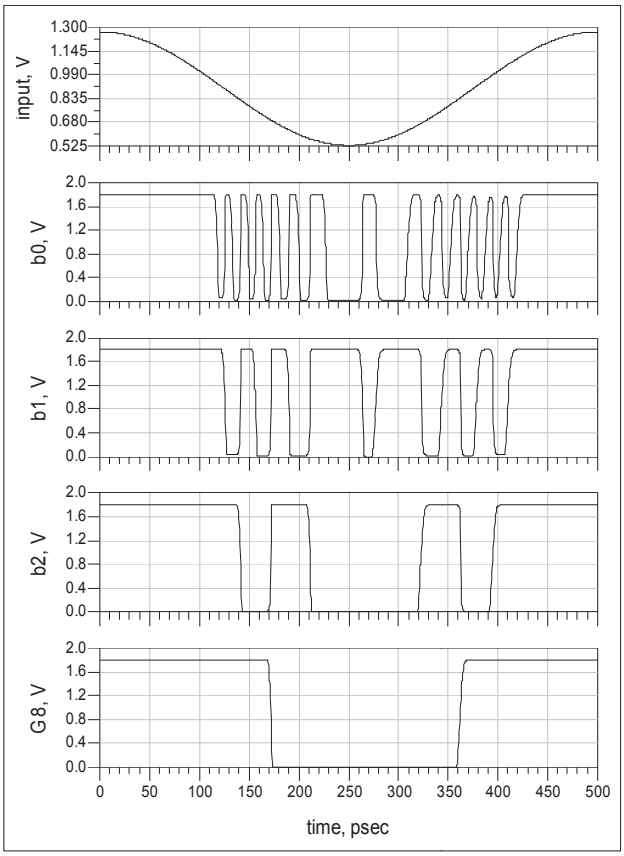

Figure 7. Transient analysis with sinusoidal input.

given below shows the DNL measurements for the design in LSBs. The simulation results for the ADC design are given in the table II given below. The transient analysis of the TIQ flash ADC was carried out and the simulation results showed that the output patterns are glitch free.

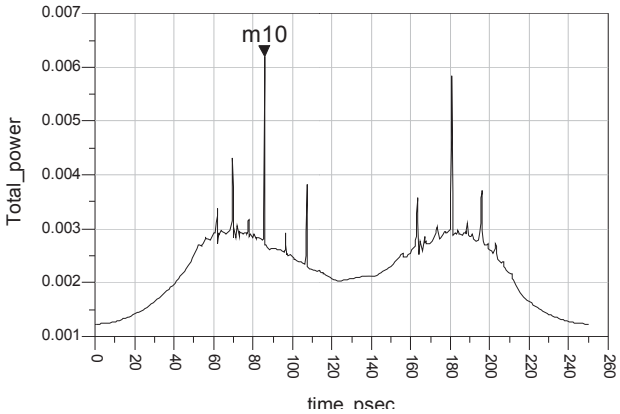

Figure 8. Power dissipation by TIQ Flash ADC with proposed encoding network.

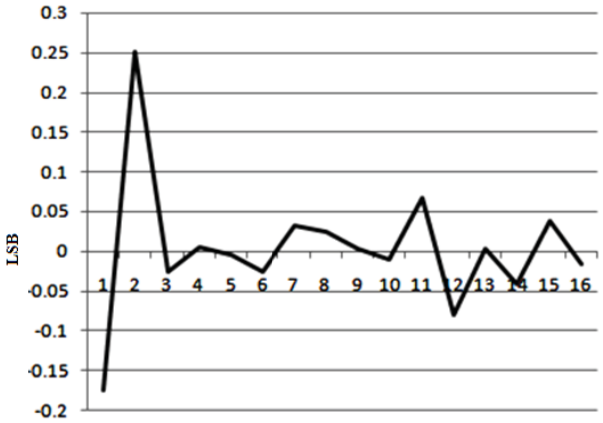

Figure 9. DNL measurments for the proposed architecture.

TABLE II. SIMULATION RESULTS OF 4-BIT TIQ FLASH ADC USING 2X1 MULTIPLEXER BASED ENCODER.

CMOS Technology	0.12 µm
Resolution	4 bits
Power Supply	1.8 Volt
Dynamic Range	500mV to 1110 mV
VLSB	0.038125 V
Power consumption	6.2031 mW
Speed	4 GS/s
DNL	-0.174 LSB to +0.256LSB
Offset error	0.5V

V. CONCLUSION.

In this paper the proposed architecture for a 4- bit Flash type ADC has been designed. A simple and fast Analog to Digital converter architecture that uses 2x1 multiplexer logic based encoder to offer higher data conversion rates is presented. The presented ADC mentains a low power consumption level as compaired to previously reported 4-bit ADCs. The presented work on ADC has a step size of 0.038125 V and uses 2x1 multiplexer based encoder network. Simulations for the transient analysis are carried out in order to measure important performance parameters. Three main ADC parameters i.e power consumed, highest conversion speed achieved and DNL were measured. Differential (DNL) errors measured are between -0.174 LSB to +0.256LSB 035676LSB. The step size i.e. VLSB is equal 0.038125 V. The ADC consumes 6.2031 mW from a 1.8V supply. Also the newly designed architecture offers a maximum speed of up to 4 Gs/s.

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