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FPGA Evaluation of Wave Front Allocator for crossbar based on-chip switches

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Abstract

Multiprocessor system-on-chip (MP-SoC) are emerging as an important trend for SoC design. Network on chip (NoC) has been proved to be efficient in handling challenging ultra-high data rates in such systems. NoC uses many high performance internetworking protocol routers that are based on crossbar switch matrix. A scheduling algorithm is used to configure the crossbar switch, deciding the order in which the packets in NoC will be routed. The scheduling algorithm must be able to keep up with the high switching rates presented by the ultra-high link rates in SoC. This paper discusses the synthesis and implementation of the Wrapped wave front allocator on varying port density request vectors. The paper will help Network-on-chip router designers to scrupulously choose the appropriate scheduler for their design.

Keywords: Network-on-chip, Arbiter, Scheduling, FPGA, Crossbar switch, Router, Wave front allocation.

1. Introduction

Multi-core system on chip based systems has provided an important design challenge for SoC designers. Moreover in order to have a complete system-on-chip integration, a significant amount of reduction in design techniques and topologies is required as the current SoC does not scale to such dimension and complexity (Banerjee, A. etal 2007). Network-on-chip has been proposed as a solution to such a problem (Sudhir N. Shelke et al 2014). NoC is basically a design paradigm that has attracted lot of attention by providing higher bandwidth and higher performance architectures for communication on chip. NoC can provide simple and scalable architectures if implemented on reconfigurable platforms (Osterloh, B. et al 2008). Network on chip

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