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Implementation of X-Y routing algorithm for NOC on reconfigurable platforms

Liyaqat Nazir* and Roohie Naaz Mir#

Computer Science Engineering
National Institute of Technology, Srinagar
Email: * liyaqatnazir_sofi@yahoo.in, # naaz310@yahoo.co.in

The communication between processing elements are suffering challenges due to power, area and latency. Temporary flit storage during communication consumes maximum power of the whole power consumption of the chip. The majority of current NoCs consume high amount of power and area for router buffers only. Removing buffers and virtual channels (VCs) significantly simplifies router design and reduces the power dissipation by a considerable amount. The Routing and arbitration scheme used in a network-on-chip based router plays a significant role in determining the performance of the whole network-on-chip based mesh. The routing algorithm unit is critical in network on chip based systems as it helps in balancing the load across the network channels even in the presence of non-uniform traffic loads. This paper presents a model for X-Y routing algorithms, the Algorithm model is implemented on FPGA platforms using arbitrary state diagram as shown in figure 2. The unique feature of this work is that it presents the synthesis and optimized implementation of the X-Y routing algorithm on FPGA platforms. The work will help NoC designers in suitable router implementation for their FPGA design.

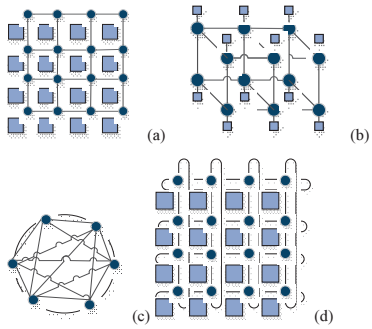

Figure 1. Block diagram of various NoC Topologies (a) 2D mesh (b)3D Mesh (c) Ring type NoC(d) Torrous NoC

The algorithm is known as Dimension order X-Y turn algorithm, which facilitates routing in two-dimensional (2D) meshes with no virtual channels. A 2D mesh has $m \times n$ nodes, where m (resp., n) is the radix of dimension x (resp., y). Each node d has an address d ;(dx, dy), where $dx \in \{0,1,2,...,m-1\}$ and $dy \in \{0,1,2,...,n-1\}$. Two nodes d: (dx, dy) and e : (ex, ey) are neighbors in dimension x (resp., y). if and only if $|dx - ex| = 1$ and $d_y = e_y$ (resp., $|dy - ey| = 1$ and $dx = ex$) In a 2D mesh, a node X is identified by a two-element vector (X_0; X_1),and node Y is identified by a two-element vector (Y_0; Y_1). Where X_0 , X_1 and Y_0, Y_1 are the coordinates of dimension 0 and dimension 1 of X, and Y directions respectively. All of the nodes that have the same coordinates of dimension 0 constitute a column, and all of the nodes that have the same coordinates of dimension 1 constitute a row. Row channels refer to channels along dimension 0; that is, a row channel connects two neighboring nodes on the same row. Similarly, column channels refer to channels along dimension 1. Further, a column channel is called an SN (respectively, NS) channel if its direction is from South to North (respectively, North to South).

A turn consists of a row channel and a column channel such that the tail node of one of the channels is the head node of the other; the common node of the two channels is called the turning node of the turn. Essentially, a turn involves a 90-degree change of traveling direction. Unless otherwise specified, a turn is a 90-degree turn in the following description..

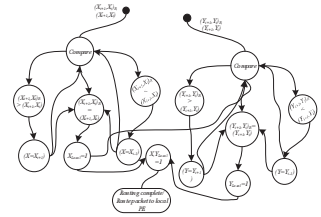

Figure 2: State diagram of Dimention order X_Y routing algorithm

Table 1: Timing comparison for Dimension order XY on Virtex 5 device

Timing Parameter	Dimension order XY routing
Maximum frequency (MHz).	551.542
Min available offset-in (ns).	1.397
Min available offset-out (ns).	3.844
Minimum period (ns)	-

Table 2: Power dissipation for Dimension order XY on Virtex 5 device.

FPGA Resource	Power dissipation (mW)
	Dimension order XY routing
Clock	2.00
Logic	.00
Signals	0.46
I/Os	0.58
Dynamic	3.04

The implementation of this work is targeted for Virtex 5 FPGA family from Xilinx.

References

1. B. Osterloh, H. Michalik, B. Fiethe, K.Kotarowski, "SoCWire: A Network-on-Chip Approach for Reconfigurable System-on-Chip Designs in Space Applications," in proc of NASA/ESA Conference on Adaptive Hardware and Systems, pp 51-56, june 2008.
2. Abdelrasul Maher, R. Mohhamed, G. Victor., "Evaluation of The Scalability of Round Robin Arbiters for NoC Routers on FPGA,"7th International symposium on Embedded Multicore/Manycore System-on-chip, pp61-66,2013.
3. Akram Ben Ahmaed, Abderazek Ben Abdallah, Kenichi, Kuroda, "Architecture and Design of Efficient 3D Network-on-Chip (3D NoC) for custom multicore SoC," in International confrence on Broadband, Wireless Computing, communication and Application, FIT,Fukuoka, Japan, Nov 2010.