

# Performance Evaluation of Different Allocation algorithms using FPGA Platforms

<sup>1</sup>Liyaqat Nazir, <sup>1</sup>Burhan Khursheed

<sup>1</sup> Computer Science Engineering.  
National Institute of Technology, Srinagar  
J&K, India.  
liyaqat\_02phd13@nitsri.net

<sup>2</sup>Roohie Naaz Mir

<sup>2</sup>Computer Science Engineering.  
National Institute of Technology, Srinagar  
J&K, India.  
naaz310@yahoo.co.in

**Abstract**—The communication between processing elements are suffering challenges due to latency. The arbitration algorithm used inside an arbitration unit of a network-on-chip based router plays a significant role in determining the performance of the whole network-on-chip based mesh. This paper reevaluates some of the standard forms of the arbitration algorithms and presents the synthesis and implementation on FPGA platforms. The work will help NoC designers to suitable allocation algorithms for their FPGA design. The implementation is carried out using various arbitration algorithms responsible for scheduling 12-bit request vector. The implementation targets Virtex5 FPGA family. The analysis concludes that the iSLIP allocation algorithm shows lower power delay product and lower resource utilization and a reasonably lower area delay product when implemented for speed optimization goal. Hence it can be best used for high speed low power NoC based systems.

**Keywords**—Network-on-chip, arbiter, scheduling, virtual channels.

## I. INTRODUCTION

In the past few years, with the concept of Network-on-Chip communication architecture, NoC has attracted lot of attention by providing higher bandwidth and higher performance architectures for communication on chip. NoC can provide simple and scalable architectures if implemented on reconfigurable platforms [1]. Network on chip offers a new communication paradigm for system on chip(SoC) design [2]. Many processing elements of SoC are connected through Network-on-chip(NoC) routers which are arranged in some regular fashion such as Mesh, linear, torrous, 2D, 3D type of topologies as shown in figure 1. To achieve high performance router should provide high band width and low latency [3]. Although the performance of the NoC is normally seen by its throughput, which is defined by the network topology, router throughput and the traffic load at the network [4]. The router throughput is determined by the critical path of the data path units in the router and the efficiency of control path units [5-8]. The data paths of the on-chip router comprises of buffers, VC and switching fabric and the control paths of on-chip communication routers are largely composed of arbiters and allocators[9]. Allocators are used to allocate virtual channels and to perform matching between a group of resources on each cycle [10-12]. As the flits/cells arriving at the fabric contend for access to the fabric with cells at both input and output A switch allocator must perform matching between the input units and the output ports of the router so that at most

one flit from each input port is selected and at most one flit destined to each output port is selected [13]. This work, therefore, focuses on the implementation of various algorithms for an allocator with low port density. The port density we selected in this work is 12-bit request vector. In this paper we carried out implementation and synthesis of various allocation algorithms used in allocators. The rest of the paper is organized as follows. Section 1 gives the introduction. Section 2 gives some background about various allocators used in NoC router. Section 3 talks about synthesis and implementation. Section 4 provides the conclusion and future scope of the work carried out and finally references are listed in the end.

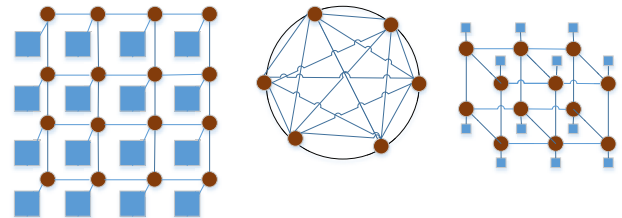


Figure1. Block diagram of various NoC topologies.

## II. ALLOCATOR

The allocator can be thought to consider the request  $R_{ij}$  and asserts the corresponding grants  $g_{ij}$ , in this way the allocator accepts an  $n \times m$  request matrix  $R$  containing the individual  $R_{ij}$  and generating a grant matrix  $G$  containing individual grants  $g_{ij}$ .  $R$  is an arbitrary binary-valued matrix.  $G$  is also a binary valued matrix that only contains ones in entries corresponding to non-zero entries in  $R$ .

$$R = \begin{bmatrix} R_{ij} & R_{ij} & R_{ij} \\ R_{ij} & R_{ij} & R_{ij} \\ R_{ij} & R_{ij} & R_{ij} \end{bmatrix} \quad G = \begin{bmatrix} R_{ij} & R_{ij} & R_{ij} \\ R_{ij} & R_{ij} & R_{ij} \\ R_{ij} & R_{ij} & R_{ij} \end{bmatrix}$$

### A. iSLIP Allocator.

iSLIP is a separable allocation method that uses round-robin arbiters and updates the priority of each arbiter only when that arbiter generates a winning grant. iSLIP can be used either in a single pass, or as an iterative matching algorithm [14]. By rotating the winning arbiters, iSLIP acts to stagger the priority of the input arbiters, resulting in fewer conflicts at the output stage [15]. The update of a priority only occurs when an