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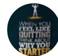
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Double Stacked Gates MOSFET Technology In both Planar as well as 3D Gate(Finfet) MOSFET's

Dual Stacked Gates In MOSFET's

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Abstract— **This paper describes the performance of a planar mosfet as well as the performance of finfet mosfet when dual gate layers are used on the same side of the mosfet channel with separate gate oxide layers, thus providing excellent control over the channel current.**

Keywords- ***Integrated circuit design; VLSI design; Nanometer technology; Dual gates; Finfet mosfet; Planar mosfet; Dual gate oxide layers; Channel control.***

I. INTRODUCTION

The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area, reduce the fabrication cost, increase operating speed and dissipate less power. Past few years have seen the introduction of nanoscale technologies for industrial production of high performance integrated circuits (IC). Also the use of dual gates will enable us to control the channel current in a more precise manner. We can use the dual gates one on the other will a layer of silicon oxide in-between to create isolation between the two gates. This will prevent leakage current losses and underutilization of channel current handling capacity [1] [2].

II. DEVELOPMENTS IN MOSFET TECHNOLOGIES

A. General Trends

The introduction of every new technology node in the past years has represented massive improvement in MOS device performance. At the transistor level, the channel length of MOS devices is automatically scaled with a new technology node. Roughly speaking, the node corresponds to half of the gate layer pitch, although the definition differs depending on the application domain. Two approaches have been introduced recently to improve transistor current capabilities:

Decreasing the oxide thickness tOX. The oxide thickness has been reduced to 1.2 nm (5 atoms). Unfortunately, the gate oxide leakage is exponentially increased, which increases the standby power consumption. Starting with the 45 nm generation, so called "metal gates" have been introduced, based on Nickel-Silicide (NiSi) [4] or Titanium-Nitride (TiN) [5], as illustrated in Fig. 1, Fig. 2(a) and (b) increasing the carrier mobility μ.

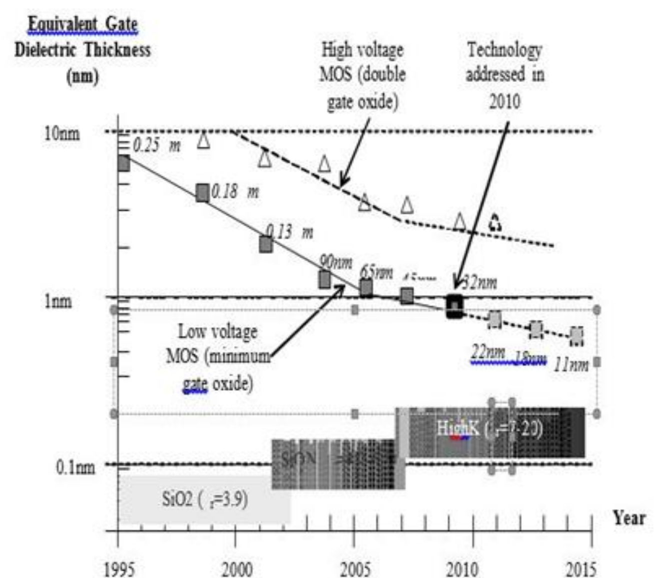

Figure 1. Technology scale down and nodes, down to 11 nm

Starting with the 90 nm generation the concept of strained silicon has been exploited to enhance the carrier mobility, which boosts both the n-channel and p-channel transistor performances. The 3rd generation of strain engineering used in the 32 nm technology massively boosts MOS performance [1] [2].

So after the introduction of dual gates on the mosfet channel, the carrier mobility will increase. We could have increased the performance of MOSFETs using single gate by providing more Vgs to the gates but that would lead to breakdown of the silicon dioxide layer and thus the MOSFET will get damaged. Using two different layers of GATE polysilicon with a layer of silicon dioxide will allow us to create a voltage field of double controllability over MOSFET channel without any possibility of breaking down the insulation.

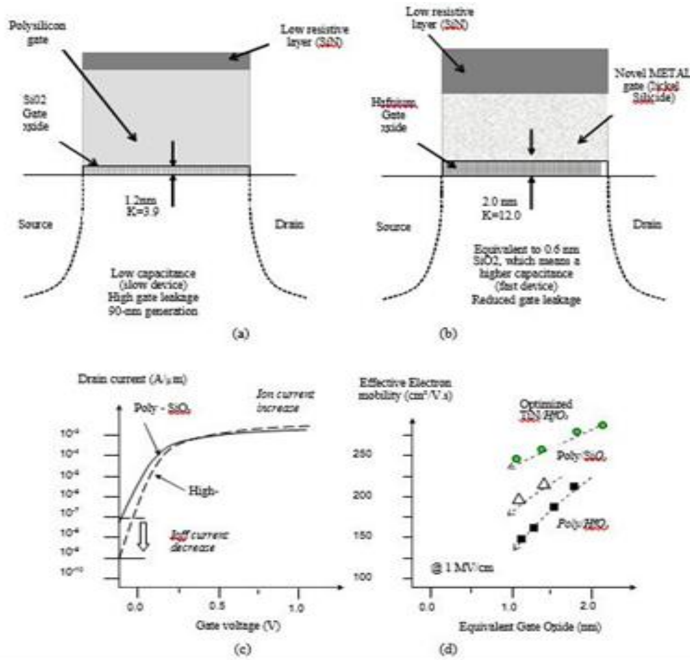

Figure 2. Compared to poly/SiO2 gates (a) the metal gate combined with High-K oxide material (b) enhances the Ion current and drastically reduces the I_{off} current (c) Electron mobility vs. Equivalent gate oxide thickness for various materials (d) from [3].

B. Approaches

The double gating of MOSFETs can be analyzed in both the planar as well as the finfet MOSFETs. The current flow in n-type MOSFET can be controlled by applying appropriate voltages on both the gate inputs. Even two different signals can be used which can result in a single MOSFET acting as a full logic gate. For example, if the voltage on one gate input is high and the other voltage is low, the low field will be created in MOSFET channel and current in channel will flow and vice versa. Thus the logic of OR gate is implemented here.

The FINFETs are already having better control over the channel conduction but they can act as perfect single monolithic logic gates by using dual stacked gates in them. Stacking of the gates will provide additional control over the current flow in the channel in case of the finfets.

III. CHALLENGES

The challenges are many in this design as we need to take care of the proper fabrication methods that would be necessary for getting the appropriate results. The masking layers need to be accounted for. Weather it would be feasible to create a silicon dioxide layer of 1nm over a polysilicon GATE layer and similar problems needs to be accounted for .The use of metal gates in the dual stacked gates might introduce problems like capacitance generation in-between the gates. The fabrication method should be feasible enough to let us get the desired dual stacked gates for a single MOSFET without compromising cost factor. The masking steps are bound to increase for the addition of a stacked gate in planar MOSFETs.

The durability of the thin silicon dioxide for insulation of the gate materials from the channel and also in-between the two gates need also to be tested. This is because the silicon dioxide does not provide a good insulation at very low thickness of <20nm.For this problem, we can use a high K-dielectric material insulators.

IV. THEORY AND OBSERVATIONS

The insulation layer that is SiO2 (gate oxide) height is taken as (x to x+5 nm) to prevent current leakage from channel to gate or vice versa.

So the gate width is also kept as (x to x+10 nm) which is a polysilicon.

Implementing dual stack gates will result in a total height of (4x nm) in both planar as well as finfet MOSFET's. This might not be feasible due to other physical constraints like pressure, etc.

So to prevent this situation, we can switch to high-k dielectric insulators and metal gates. High-k [6][7] dielectrics provides excellent insulation at very low heights and metal gates provide excellent control over the channel. We have replaced Sio2 with (high kappa) dielectric insulators and polysilicon gates with metal (aluminum or copper) gates. This now helps us in maintaining very low overall structure height of the MOSFET without any compromise on the performance.

Now, the metal gates are of the height of (x/2 to x+5/2) still providing excellent and better control over the channel as compared to polysilicon gates. The height of (high-k) dielectric can also be kept at (x/2 to x+5/2) which is a positive feature. By implementing dual stack gates, we will get a total height of (2x nm) which is just half of what we had in earlier case.

The fabrication process is also feasible for dual stacked gates as we are not changing any core design of the MOSFET, although the masking steps will increase.

Features of Using Dual Stacked gates in MOSFET's:

1. A single MOSFET can act as an OR logic gate.
2. Better control over the channel.
3. Increased uniformity in the applied voltage field.
4. Power dissipation will decrease due to decrease in (Ron) of MOSFET.
5. Rise time and fall time during the MOSFET operation will decrease due to decrease in effective gate capacitance i.e.

$$C_{effective} = \frac{1}{C_{ox1}} + \frac{1}{C_{ox2}}$$

6. Overall performance characteristics will get better.
7. A second gate control can also act as a standby controller for channel in case the first gate short circuits with the channel.
8. We can create a optimum level of control over the channel by varying both the gate voltages to different values as per the requirement.

Figure 3. Poor Voltage Control in Planar MOSFET using Single Gate Control

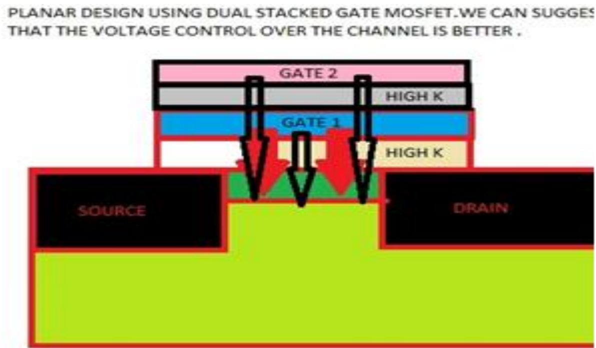

Figure 4. Better Voltage Control Using Dual Stacked Gates in Planar Design

FINFET DESIGN USING SINGLE GATE MOSFET

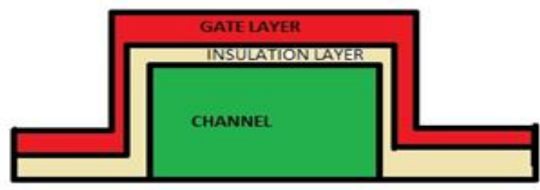

Figure 5. Poor Voltage Control in Finfet MOSFET using Single Gate Control (Cross Sectional View)

FINFET DESIGN USING DUAL STACKED GATES IN MOSFET.WE CAN SUGGEST THAT THE VOLTAGE CONTROL OVER THE CHANNEL IS BETTER.

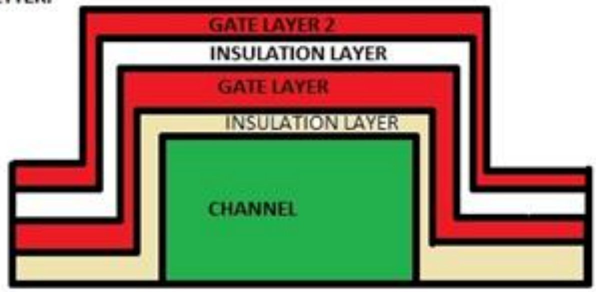

Figure 6. Better Voltage Control Using Dual Stacked Gates in Finfet Design MOSFET (Cross Sectional View)

V. ANALYTICAL RESULTS

We know that for a single gate MOSFET, the general equation for the Drain Current is given by:

$$I_D = \mu_n C_{OX} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2 \quad (1)$$

Also, after implementing the dual stacked gates, this equation will become:

$$I_D = \mu_n[\frac{1}{C_{OX1}} + \frac{1}{C_{OX2}}]\frac{W}{L} [(V_{GS1} + V_{GS2}) - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2 \quad (2)$$

Also, the equation for maximum drain current in a single gate MOSFET is governed by the following equation:

$$I_{D,max} = \frac{1}{2}\mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (3)$$

Equation (3) determines the drain current for saturation region of MOSFET operation.

After implementing the dual stacked gates, the equation for maximum drain current will become:

$$I_{D,max} = \frac{1}{2}\mu_n[\frac{1}{C_{OX1}} + \frac{1}{C_{OX2}}] \frac{W}{L} [(V_{GS1} + V_{GS2}) - V_{TH})^2 \quad (4)$$

Equation (4) will determine the drain current for saturation region of MOSFET operation in a dual stacked gate design.

For deep triode region of operation in a single gate MOSFET design, the drain current is given by:

$$I_D \approx \mu_n C_{OX} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} \quad (5)$$

When we implement the dual stacked gates MOSFET design, the equation becomes:

$$I_D \approx \mu_n \left[\frac{1}{C_{OX1}} + \frac{1}{C_{OX2}}\right]\frac{W}{L}[(V_{GS1} + V_{GS2}) - V_{TH})]V_{DS} \quad (6)$$

Now, for the ON resistance value of the MOSFET channel in a single gate MOSFET design, we have:

$$R_{on} = \frac{1}{\mu_n C_{OX} \frac{W}{L} [(V_{GS} - V_{TH})]} \quad (7)$$

After implementing the dual stacked gated design, we get the following value for ON resistance:

$$R_{on} = \frac{1}{\mu_n \left[\frac{1}{C_{OX1}} + \frac{1}{C_{OX2}}\right]\frac{W}{L}[(V_{GS1} + V_{GS2}) - V_{TH})]} \quad (8)$$

For the figure of merit of the single gate MOSFET design, we have:

$$g_m = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH}) \quad (9)$$

After implementing the dual stacked gate design in MOSFET, we get:

$$g_m = \mu_n C_{OX} \frac{W}{L} \{(V_{GS1} + V_{GS2}) - V_{TH}\} \quad (10)$$

The relation between figure of merit and drain current in a single gate MOSFET design is given by:

$$g_m = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_D} \quad (11)$$

Also, the relation between figure of merit and drain current in a dual stacked gate MOSFET design is given by:

$$g_m = \sqrt{2\mu_n \left[\frac{1}{C_{OX1}} + \frac{1}{C_{OX2}}\right] \frac{W}{L} I_D} \quad (12)$$

The relation between gate voltage, drain current and figure of merit in a single gate MOSFET is given by:

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}} \quad (13)$$

The relation between gate voltages, drain current and figure of merit in a dual stacked gates MOSFET design is given by:

$$g_m = \frac{2I_D}{(V_{GS1} + V_{GS2}) - V_{TH}} \quad (14)$$

So we see that by implementing dual stacked gates in a MOSFET, we get increased value of Drain Current Id which is a good point and this is due to the effect of Vgs2, which is a second voltage control gate (second stacked gate).We also see that the implementation of dual stacked gates lead to the decrease in the overall capacitance value due to insulation dielectrics. The value of capacitance Cox1 and Cox2 is in pico-farad (10-12) range i.e. the MOSFET feature is tiny (<100nm).So the effect of Cox1 and Cox2 in (2), (4), (6), (8), (10), (12) is very less as compared to the effect of Vgs2 in the said equations. The voltage control on Vgs1 as well as Vgs2 is in volts range. Thus

$$Effective \left[\frac{1}{C_{ox1}} + \frac{1}{C_{ox2}}\right] \ll Effective\ (V_{gs1} + V_{gs2})$$

Another thing that we observe is that the value of Ron decreases by implementing stacked gates. We know that, more less the value of Ron, the better it is as the power dissipation will also decrease/be less.

The trans-conductance also increases by implementing dual stacked gates in a MOSFET as seen in (14).

References

[1] S. Natarajan and al. "A 32nm Logic Technology Featuring 2nd-Generation High-k+ Metal-Gate Transistors, Enhanced Channel Strain", Proceedings of IEDM 2008.

[2] C. X. Chen et al, “A Cost Effective 32nm High-K/ Metal Gate CMOS Technology for Low Power Applications with Single-Metal/Gate-First Process”, Symposium on VLSI, 2008, pp. 88-89.

[3] T. A. Hudson, E. R. Doering and L.T. Gwen, “Teaching mixed-signal integrated circuit design to undergraduates,” IEEE Trans. Education, vol. 49, no. 1, pp. 39 – 48, Feb. 2006E. Sicard. Microwind & Dsch user's manual version 3.5 on-line at http://www.microwind.org

[4] C Lavoie, FM d'Heurle, C Detavernier- Microelectronic …, 2003 - Elsevier_http://www.sciencedirect.com/science/article/pii/S0167931703003800

[5] NC Saha, HG Tompkins - Journal of Applied Physics, 1992 - scitation.aip.orghttp://scitation.aip.org/content/aip/journal/jap/47/4/10.1063/1.322842

[6] MV Fischetti, DA Neumayer… - Journal of Applied …, 2001 - adsabs.harvard.edu_http://adsabs.harvard.edu/abs/2001JAP....90.4587F

[7] J Xiang, W Lu, Y Hu, Y Wu, H Yan, CM Lieber - Nature, 2006 - nature.com_http://www.nature.com/nature/journal/v441/n7092/abs/nature04796.html

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