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Singular perturbation-based model reduction of power electronic circuits

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Abstract: Here, the authors present a model order reduction (MOR) framework based on singular perturbation approximation to accelerate the simulation of high-fidelity power electronic converters. The problem of slow simulation speeds caused due to the wide span of the eigenvalues is mitigated by implementing the proposed framework. The dynamics of the original stiff system is approximated by neglecting the transient contribution of the non-dominant eigenvalues and retaining the steady-state contribution of all the eigenvalues of the system. The model reduction problem has been reformulated to fit the switched nature of these circuits. An error bound for the approximation method has been derived. The method is demonstrated on a DC–DC boost converter and a Class-E amplifier. Significant improvement in speed and reduction in the size of the solution arrays is achieved. It is seen that the reduced-order models are able to replicate the response of the original models and the approximation error is within acceptable limits.

1 Introduction

To minimise repetitive breadboarding and design alterations of power electronic circuits, accurate simulation is essential. The goal is to evaluate the performance of power electronic circuits using software for precise prediction of complex phenomena such as parasitic effects, electromagnetic interference, thermal, and mechanical effects etc. The demand for accurate simulation is further escalated during the design optimisation process where many iterations are required to be performed such that the design constraints are satisfied and the target performance is met. This prevents unnecessary cost escalations and helps in getting the hardware prototype ready in the first attempt [1, 2].

Simulation of power electronic circuits throws up a different set of challenges not normally encountered while simulating their digital circuit counterparts. Comparing the two, it is seen that for the same size, while the schematic of the former is simpler, the complexity of the layout and analysis is far more complicated than the latter [3].

A characteristic feature distinguishing power electronic circuits is the highly non-linear behaviour of the switching devices employed in power electronic circuits. These non-linearities are mathematically *stiff*; the time constants span several orders of magnitude. The capacitors and inductors of the power stage have significantly larger time constants compared to the conversion period. On the other hand, time constants of transient shaping components such as snubbers are much smaller. The wide span of time constants is challenging in the sense that to capture the fastest transients, an extremely small time-step has to be taken to ensure the stability of the numerical method used in the simulation. Due to the presence of elements with large time constants, it is essential that the simulation continues until the circuit reaches steady state, which may well be a few hundred or more conversion periods. To effectively capture the effects of all the elements of the circuit, the simulation must run for a long time, albeit with sufficiently small time steps. The stiffness of the system rules out the use of fixed step-size solvers such as Euler, Runge–Kutta (RK) etc [4]. For solving such systems, variable step-size methods have to be used. The characteristic feature of these methods is the ability to change the step-size of the integration during the course of the solution. For the solution of fast-evolving eigenvalues, a small step-size has to be chosen to ensure numerical accuracy and stability [5]. This step-size is based on the estimated error at that particular step. Once the transients die down, the step-size is gradually increased, maintaining the error within limits. The step-size, however, cannot be increased without bound. This upper limit is set due to the periodic excitation of the switching transients [6]. In addition, the transition of the switches from *on* to *off* and vice-versa has to be determined accurately. This accuracy has to be of the order of 10^{-4} or higher, which otherwise may lead to oscillation in the solution [7]. This nullifies the advantages of the variable step-size methods. The simulation of the complete response of power electronic circuits by conventional simulation tools turns out to be computationally prohibitive and inefficient [8].

Power electronic circuits are highly sensitive to parasitic effects arising from the actual layout of the circuit board. Even though the elements producing these effects are absent in the circuit schematic, they critically influence the actual behaviour of the circuit. For accurate simulation, high-fidelity models incorporating effects such as stray parasitics, electromagnetic interference etc. have to be developed. Naturally, this leads to an increased complexity in obtaining an analytical solution of the circuit. The requirement of computational resources also increases.

Although some attempts have been made to simplify power electronic circuit simulation [6, 8–12], the problem remains largely unaddressed. To accelerate the speed and to reduce the computational resources needed for the simulation, model order reduction (MOR) can be used [13]. MOR aims at approximating a given large-scale system (LSS) with a reduced order system such that the input-output relation of the system is preserved. MOR methods have been extensively researched and successfully applied to a wide variety of LSS such as circuits and interconnects, microelectromechanical systems (MEMS), turbomachinery, control design, computational electromagnetics, and VLSI circuits. See [14, 15] for an elaborate survey on applications of MOR. Despite their popularity, works on the application of MOR methods on power electronic circuits are rather limited. A discrete-time state-space model based on the sampled-data modelling approach has been proposed in [16]. Assuming a generalised discontinuous current and voltage mode (DCVM), the continuous mode (CM), discontinuous current mode (DCM), and the discontinuous voltage mode (DVM) are derived as special cases. Reduced-order models are then derived using Principal Component Analysis (PCA) from the balanced realisation of the system. It is shown that order