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IFAC PapersOnLine 51-1 (2018) 273–278

Simulation Acceleration of High-Fidelity Nonlinear Power Electronic Circuits Using Model Order Reduction

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Abstract: In this paper, we present a Model Order Reduction (MOR) framework to enhance the simulation speeds of switched high-fidelity power electronic circuits with nonlinear inductors. The nonlinear inductor is modeled as a piecewise linear element. The problem of prohibitively slow speeds of the simulation caused due to the wide span of the eigenvalues is mitigated by implementing the proposed framework. Dynamics of the original stiff system is approximated by a nonstiff reduced order system by retaining the dominant modes of the system. The method is demonstrated on a DC-DC boost converter with a saturated inductor. Significant improvements in simulation speed and considerable reduction in size of the solution arrays is achieved.

Keywords: Model Order Reduction, power electronics, circuit simulation, high-fidelity modeling

1. INTRODUCTION

In order to reduce design alterations and repetitive breadboarding of power electronic circuits, an accurate simulation strategy is essential. This helps in getting the hardware prototype ready in the first attempt and also minimizes unwanted cost escalations (Mohan et al., 1994). Compared to digital circuit simulation, the simulation of power electronic circuits throws up an altogether different set of challenges. It is seen that for the two circuit types of the same physical size, the complexity of power electronic circuits far exceeds that of their digital circuit counterparts (Wilson, 1988).

A distinguishing feature is the highly nonlinear behavior of the switching devices used in power electronic circuits. These nonlinearities are mathematically *stiff*: their time constants span several orders of magnitude. While inductors and capacitors of the power stage have significantly large time constants in comparison to the conversion period, time constants of transient shaping components such as snubbers are much smaller. This wide span of the eigenvalues is especially challenging in the sense that to capture the fastest transients, an exceedingly small time-step has to be taken to ensure stability of the numerical method used in the simulation. However, the simulation must continue till the system reaches its steady state. This may well be a few hundred or more conversion periods, owing to the presence of elements with large time constants. Therefore, to capture effects of all the elements of the circuit, the simulation must run for a long time, albeit with sufficiently small time-steps.

The use of fixed step-size integration routines such as Euler, Runge-Kutta (RK) etc. is naturally ruled out due the stiffness of the system. Even with stiff solvers using variable step-size such as numerical and backward differentiation formulas (NDFs) and (BDFs) (Shampine and Reichelt, 1997), the simulation is still slow as the step-size cannot be changed without bound. An upper limit on the step-size is set by the magnitude of transients in the circuit. Also, the transition of the switches from *on* to *off* and vice-versa needs to be determined with an accuracy of the order of 10^{-4}, which otherwise leads to oscillation in the solution (Wong et al., 1984).

Power electronic circuits are highly sensitive to parasitic effects arising due to the physical layout of the elements on the circuit board. Even though the elements producing these effects are absent in the circuit schematic, they critically alter the actual behavior of the circuit. For accurate simulation, it is thus required that detailed high-fidelity models incorporating effects such as stray parasitics and electromagnetic interference be developed. This naturally leads to increased complexity in obtaining the analytical solution of the circuit variables. Computational resources required for solving such systems also increase.

Even though some attempts have been made in the past to address some of the issues in power electronic circuit simulation, the problem continues to remain unaddressed, see White and Leeb (1991), Maksimovic (1997), Sun and Grotstollen (1997), Felder and Rembold (2003), Pekarek et al. (2004), Lian and Lehn (2012), Kato et al. (2009), Khan et al. (2017), Khan et al. (2018). To enhance the simulation speed and to reduce the computational re-

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10.1016/j.ifacol.2018.05.069