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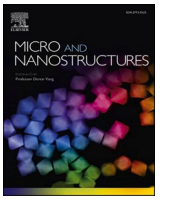

A review: ON-state enhancement by empirical insights and material analysis (Si,Ge, III-V) for various TFETs

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ABSTRACT

The Tunnel Field Effect Transistor (TFET) has emerged as a prominent alternative to customary MOSFETs (Metal Oxide Semiconductor Field Effect Transistor), especially for low-power applications in the deep submicron regime. While the latter endure from increased short-channel effects, leakage currents, and a minimum subthreshold swing (SS) limit of 60 mV/dec at room temperature, the former offer perks, such as ultra-low leakage current and the potential to achieve SS below 60 mV/dec due to their band-to-band tunnelling (BTBT) phenomenon. However, TFETs face key challenges, including low ON-state current (Ion) and ambipolar conduction. This comprehensive review explores structural innovations and design techniques aimed at enhancing the ON-state performance and minimizing ambipolarity. Various TFET architectures—such as p-i-n, junctionless, dual-gate, heterojunction and nanowire configurations-are critically examined, including material-oriented, specifically Si, Ge and III-V. This manuscript also emphasizes the impact of physical parameter variations on device and RF characteristics, on the basis of empirical approach to achieving a higher I_{on}/I_{off} ratio and enabling Tunnel FETs to serve as viable replacements for MOSFETs in future IC technologies.

1. Introduction

Multiple second-order effects, including channel length modulation, drain-induced barrier lowering (DIBL), and hot carrier injection, considerably degrade device performance, and they have been implemented due to the ongoing shrinking of conventional MOSFETs as semiconductor technology moves into the sub-nanometer regime. Furthermore, further power scaling is not practical since MOSFETs possess subthreshold swing (SS) $<$ 60 mV/dec at ambient temperature as an outcome of the Boltzmann regime. Fig. 1 portrays the evolution of nanoscale devices from the base.

These limitations have sparked extensive research into novel device architectures that can sustain performance scaling. The Tunnel Field Effect Transistor (TFET) has gathered an abundance of priority since it can get approximately the SS limit through a band-to-band tunnelling (BTBT) mechanism [1–3]. Alternatives include impact ionisation devices, suspended gate FETs, and nanowire-based MOSFETs. TFETs have certain good qualities that make them good for future low-power integrated circuits. These include lower power dissipation, less leakage current, and steeper subthreshold slopes. But there are issues such as lessened ON-state current (I_{ON}) and ambipolar conductivity. To refine ON-state performance and reduce ambipolarity, researchers have offered an assortment of intriguing structures and materials, including dielectric pockets, heterojunctions, gate-source overlaps, and junctionless designs.

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